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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/688,203	10/16/2000	Kenichiro Nakagawa	NEC00P264-ks	8790

7590 01/16/2002

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EXAMINER	
COLLINS, DEVEN M	
ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 01/16/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/688,203	NAKAGAWA, KENICHIRO	
	Examiner	Art Unit	
	D. M. Collins	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 December 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) *7-12* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Election/Restriction

1. Applicant's election without traverse of Group II, claims 1-6 in Paper No. 4 is acknowledged.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-6 are rejected under 35 U.S.C. 102(b) as being unpatentable over Shimizu et al. (5,683,923, dated 11/4/97).

Shimizu et al. show the method as claimed in the Figures 1-64 with corresponding text. In re claim 1, Shimizu disclose a method of manufacturing a semiconductor memory device capable of electrically writing and erasing data, said semiconductor memory device (figs. 1, 2) having a plurality of cell transistors 9 for storing data, each of said cell transistors having a floating gate

electrode 5 and a control gate electrode 7, and a plurality of select transistors for controlling and selecting said cell transistors 9, said method comprising the steps of:

before forming the control gate electrodes 7 of said cell transistors, exposing a surface of a substrate 1 directly above channel regions 14 of said select transistors fabricated in the same process as the cell transistors 9;

forming gate insulating films 11 of said select transistors on the exposed surface of the substrate 1; and

forming the control gate electrodes 7 of said cell transistors and forming gate electrodes of said select transistors on said gate insulating films 11.

In re claim 2, Shimizu disclose the method of manufacturing a semiconductor memory device (figs. 1, 2) according to claim 1, further comprising the step of:

simultaneously forming a first diffused layer serving as source 10 and drain 9 regions of said cell transistors and a second diffused layer serving as source and drain regions of said select transistors.

In re claim 3, Shimizu disclose the method of manufacturing a semiconductor memory device (figs. 1, 2) according to claim 1, further comprising the steps of:

forming gate insulating films 11 of transistors of a peripheral circuit comprising a logic operation circuit (col. 17, par. 2), simultaneously with the gate insulating films 11 of said select transistors;

and forming gate electrodes (5, 7) of the transistors of said peripheral circuit simultaneously with the gate electrodes of said select transistors.

In re claim 4, Shimizu disclose

the method of manufacturing a semiconductor memory device (figs. 1, 2) according to claim 2, further comprising the steps of:

forming gate insulating films 11 of transistors of a peripheral circuit comprising a logic operation circuit, simultaneously with the gate insulating films 11 of said select transistors;

and forming gate electrodes (5, 7) of the transistors of said peripheral circuit simultaneously with the gate electrodes of said select transistors.

In re claim 5, Shimizu disclose the method of manufacturing a semiconductor memory device (figs. 1, 2) according to claim 3, wherein the gate insulating films 11 of said select transistors have a film thickness which is the same as the film thickness of the gate insulating film of a transistor which requires a high withstand voltage, among the transistors of said peripheral circuit.

In re claim 6, Shimizu disclose the method of manufacturing a semiconductor memory device (figs. 1, 2) according to claim 4, wherein the gate insulating films 11 of said select transistors have a film thickness which is the same as the film thickness of the gate insulating film 11 of a transistor which requires a high withstand voltage, among the transistors of said peripheral circuit.

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Examiner Deven M. Collins whose telephone number is (703) 305-7840. The examiner can normally be reached on Monday-Friday from 6:30 AM to 3:00 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M Fahmy, can be reached on (703) 308-4918. The fax phone number for this Group is (703) 305-3432.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-0956.

DMC

January 14, 2002

Wael Fahmy

SUPERVISORY PRIMARY EXAMINER
TECHNOLOGY CENTER 2800